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(54) Method of forming a metallization film containing copper on the surface of a semiconductor device.

(57) A method of producing a semiconductor device comprises the steps of forming a metallization film (18) including copper on a surface of a substrate (10,12,14,16), and depositing an insulating film (20) on the surface including the metallization film at a temperature which is lower than an oxidation temperature of copper.

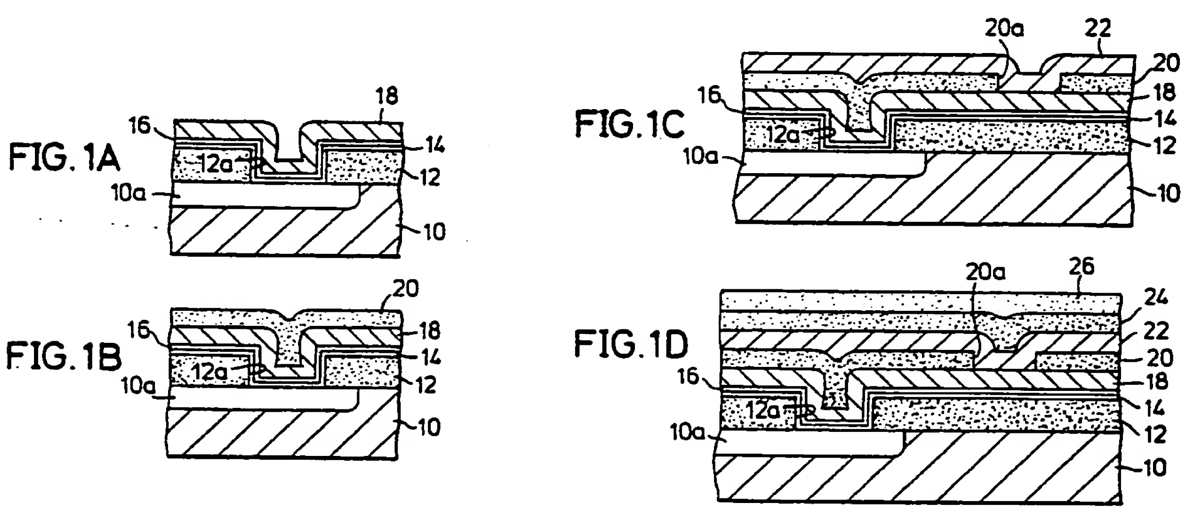

FIG. 1A

FIG. 1B

FIG. 1C

FIG. 1D

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METHOD OF PRODUCING SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

The present invention generally relates to methods of producing semiconductor devices, and in particular to methods of producing semiconductor devices using copper or copper alloy as a wiring or metallization material.

As well known, a metallization pattern of a large scale integrated circuit (LSI) diminishes in width as its integration density increases. Although aluminum (Al) metallization is widely used for semiconductor chips, its width for metallization is limited to the range of 0.5 to 0.6 μm. This is because the electromigration increasingly occurs as the aluminum metallization pattern becomes narrower. For these reasons, the use of a metallic material of a high melting point such as molybdenum (Mo) of tungsten (W) in replace of Al is considered. However, the resistivity of Mo or W is approximately twice the resistivity of Al in bulk and is more in a thin film. Therefore, a metallization material having a high electromigration resistance and a low resistivity is currently being investigated.

Presently, copper (Cu) is being investigated for metallization of LSIs due to its better electromigration resistance and lower resistivity than Al. A conventional semiconductor device with copper metallization is designed so that a copper metallization film is directly deposited on an insulating film such as silicon dioxide (SiO_2) which is deposited on a silicon (Si) substrate and over contact holes formed in the insulating film so as to be positioned on diffused layers formed in the Si substrate. Of course, the copper film is patterned in accordance with the wiring pattern.

The semiconductor device thus configured is generally annealed at a high temperature of the order of 400°C or over in order to grow grains of Cu and thereby improve the electromigration resistance. Thereafter, an insulating film is deposited on the Cu metallization film as well as the insulating film. The deposition of the insulating film is conventionally carried out by a chemical vapor deposition (CVD) at a temperature of approximately 420°C. The insulating film on the copper metallization film may be made of, for example, phosphosilicate glass (PSG), silicon nitride (Si_3O_4) or SiO_2. The insulating film acts as a passivation film or a layer-to-layer insulating film in multilevel interconnections.

However, there are disadvantages with the conventional method of producing semiconductor device with the Cu metallization mentioned above. That is, the oxidation temperature of Cu ranges of 200 to 250°C, whereas the heat treating temperature in the CVD is of the order of 400 C or over. Therefore, Cu in the metallization film is easily oxidized due to oxygen which exists in an ambient atmosphere when depositing the insulating film by the CVD process. Oxidation of Cu damages the surface of the metallization film which is in contact with the insulation film and therefore degrades the Cu metallization film especially in terms of the resistance.

SUMMARY OF THE INVENTION

Accordingly, a general object of the present invention is to provide a novel and effective method of producing a semiconductor device, in which the above problems have been eliminated.

A more specific object of the present invention is to provide a method of producing a semiconductor device, in which oxidation of a metallization film including at least copper is effectively prevented and its metallization resistance can be kept low even after deposition of an insulating layer.

To attain the above-mentioned objects and features, according to the present invention, there is provided a method of producing a semiconductor device comprising the steps of forming a metallization film including copper on a surface of a substrate, and depositing an insulating film on the surface including the metallization film at a temperature which is lower than an oxidation temperature of copper.

Other objects and further features of the present invention will be apparent from the following detailed description when read in conjunction with the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS.1A through 1D are respectively cross sectional views for explaining an example of a method of producing a semiconductor device according to the present invention; and

FIG.2 is a graph for explaining effects provided by the present invention.

DETAILED DESCRIPTION

A description will be given of an embodiment of a method of producing a semiconductor device according to the present invention by referring to FIGS.1A through 1D. As will become apparent from a description provided hereinafter, FIGS.1A and 1B show producing steps with respect to a first-level Cu metallization film, FIGS.1C and 1D show producing steps with regard to a second-level Cu metallization film.

Referring to FIG.1A, an insulating film 12 is deposited on the top surface of a silicon substrate 10, in which there is formed an n^+-diffused layer 10a. The insulating film 12 may be silicon dioxide (SiO_2), phosphor-silicate glass (PSG) or silicon nitride (Si_3N_4). The width of the insulating film 12 is 4,000Å, for example. Then, a metallic layer 14 is deposited on the top of the n^+-diffused layer 10a. The metallic layer 14 may be made of Ti, Al or platinum (Pt). The deposition of the metallic layer 14 may be carried out by a D.C. magnetron sputtering method. When using Ti, for example, a Ti target is sputtered in argon (Ar) gas at a pressure of 5mTorr with a power of D.C.2kW. The film thickness of the metallic layer 14 is preferably in the range of 100Å to 1,000Å. The metallic layer 14 is provided to form an ohmic contact to the Si substrate 10. This is because when using Ti, for example, titanium silicide ($TiSi_2$) which is produced by the application of heat makes a low-resistance contact.

Next, a barrier layer 16 is deposited on the metallic layer 14. The barrier layer 16 has the same pattern as a Cu metallization layer 18, which will be described in detail later. In other words, the barrier layer 16 underlies the Cu metallization layer 18. The barrier layer 16 prevents the reaction and interdiffusion between the Cu metallization film 18 and the Si substrate 10 and also between the former and the insulating film 12. In detail, the barrier layer 16 prevents not only the Cu atoms from diffusing into the Si substrate 10 and the insulating film 12 but also the Si atoms from migrating to the Cu metallization film 18. The barrier layer 16 may be made of titanium nitride (TiN), tungsten (W), tungsten nitride (WN), zirconium nitride (ZrN), titanium carbide (TiC), tungsten carbide (WC), tantalum (Ta), tantalum nitride (TaN) or titanium tungsten (TiW). The film thickness of the barrier layer 16 is preferably in the range of 500Å to 3,000Å. The barrier layer 16 may be deposited by means of a reactive magnetron sputtering method. For example, a target of Ti is sputtered in $Ar + N_2$ gas at a pressure of 5mTorr with a power of D.C.4kW.

Thereafter, the Cu metallization film 18 is deposited on the barrier layer 16. The Cu metallization film 18 may be deposited by means of the D.C. magnetron sputtering method. For example, a target of Cu is sputtered in Ar gas at a pressure of 5mTorr with a power of D.C.2kW. The film thickness of Cu is preferably in the range of 3,000Å to 2µm. It is also possible to use in replace of Cu, alloy of Cu such as Cu-Ti or Cu-Zr as a material forming the metallization film which is to be deposited on the diffusion barrier layer 16.

The metallic layer 14, the barrier layer 16 and the Cu metallization film 18 are patterned in accordance with a wiring pattern. Patterning these layers may be performed by the following steps. First, a mask layer of PSG or TiN, for example, is deposited on the top of the Cu metallization film 18 by reactive magnetron sputtering method. Secondly, a resist is patterned on the top of the mask layer. Then, the mask is etched off by a reactive ion etching process. Thereafter, the resist ashing is carried out. Next, the Cu metallization film 18 is etched off and thus patterned by an ion milling process. Finally, the underlying metallic layer 14 and the barrier layer 16 are etched off together with the mask by the reactive ion etching process.

The structure thus produced is illustrated in FIG.1A.

The next step is illustrated in FIG.1B. A layer-to-layer insulating film 20 is deposited over the top surface of the structure shown in FIG.1A including the Cu metallization layer 18. In this deposition, it is important to grow the layer-to-layer insulating film 20 at a temperature lower than 200°C. This process may be carried out by radio frequency (RF) sputtering, plasma-assisted chemical vapor deposition (PCVD) or electron cyclotron resonance (ECR) PCVD. When using the RF sputtering or PCVD, SiO_2, PSG or Si_3N_4 may be employed as a material of the layer-to-layer insulating layer 20, whereas when using the ECR-PCVD, SiO_2 or Si_3N_4 may be used. TABLES I, II AND III are respectively shown which denote examples of each deposition method mentioned-above.

TABLE I (RF-SPUTTERING)

Material	Gas ; Temp.	Power; Pressure
SiO_2	Ar; 100-180°C	Rf 2kW; 1.7 x 10^{-3} Torr
PSG	Ar; 100-180°C	Rf 2kW; 1.7 x 10^{-3} Torr
Si_3N_4	Ar; 100-180°C	Rf 2kW; 1.7 x 10^{-3} Torr

TABLE II (PCVD)

Material	Gas ; Temp.	Power; Frequency; Pressure
SiO_2	SiH_4(6cc)+ N_2O(300cc)+ N_2(54cc); 200°C Growth	Rf 35W; 200kHz; 1Torr
PSG	1%PH_3(50cc)+ N_2(50cc); 200°C Growth	Rf 35W; 200kHz; 1Torr
Si_3N_4	SiH_4(25cc)+ NH_3(100cc)+ N_2(200cc); 200°C Growth	Rf 35W; 200kHz; 1Torr

TABLE III (ECR-PCVD)

Material	Gas & Temp.	Power; Frequency; Pressure
SiO_2	SiH_4(20cc) +O_2(40cc); 150°C Growth	Rf 1kW; 2.45GHz; 1mTorr
Si_3N_4	SiH_4(10cc) +N_2(30cc); 150°C Growth	Rf 400-500W; 2.45GHz; 1mTorr

It will become apparent from the above tables that the temperature during the deposition process is kept lower than 200°C which is a limit where Cu is oxidized. It is therefore possible to prevent an increase in the resistanc of the Cu metallization film 18.

When configuring a multilevel interconnection, a through hole 20a is formed in the layer-to-layer insulating film 20. Then, Cu is metallized over the layer-to-layer insulating film 20, so that a Cu metallization film 22 is formed. This deposition may be carried out by the D.C. magnetron sputtering method. The thickness of the Cu metallization film 22 is preferably in the range of 3,000Å to 2µm. Thereafter, the Cu metallization film is patterned by the reactive ion etching. Then, an insulating film 24 is deposited by means

of one of the methods described in relation to the deposition of the insulating film 20. Finally, an insulating cover film 26 is deposited on the insulating film 22. In this deposition, even the CVD may be employed, because the second-level Cu metallization film 22 is totally covered by the insulating film 24. The combination of materials of the insulating films 20, 24 and 26 is arbitrary. For example, it is possible to form the insulating films 20, 24 and 26 with SiO_2, PSG, PSG and Si_3N_4, respectively.

FIG.2 shows the experimental results of the measurement of the resistivity (μΩm) of four types of semiconductor devices. A first type of a semiconductor device has a structure without an insulating film on the Cu metallization film as shown in FIG.1A. A second type has a structure in which a CVD-PSG is deposited on the Cu metallization film. A thir type has a structure in which a CVD-Si_3N_4 is deposited on the Cu film. A fourth type has a structure in which a RF sputter-PSG is deposited on the Cu metallization film. The resistivity was plotter for each sample before the annealing and after the annealing at 450°C for 30 minutes. The experimental results clearly show that the RF sputtering which is one of the deposition methods for the insulating film is extremely effective to prevent an increase in the resistivity of the Cu metallization film even when the 450 C annealing is carried out. On the other hand, conventional CVD method already causes an increase of the resistivity even before the annealing. Therefore, a further increase in the resistivity due to the annealing is easily guessed. For this reason, in the experiment, the resistivity measurement regarding the CVD-PSG and CVD-Si_3N_4 was not performed.

The present invention is not limited to the embodiments, but various variations and modifications may be made without departing from the scope of the present invention.

Claims

1. A method of producing a semiconductor device comprising the steps of forming a metallization film (18) including copper on a surface of a substrate (10,12,14,16) and depositing an insulating film (20) on said surface including said metallization film, characterized in that said step of depositing said insulating film (20) is performed at a temperature which is lower than an oxidation temperature of copper.

2. A method of producing a semiconductor device as claimed in claim 1, characterized in that the temperature at said depositing step is 200°C or lower.

3. A method of producing a semiconductor device as claimed in any of claims 1 and 2, characteriz d in that said method further comprises the step of annealing said semiconductor device having said insulating film deposited on said substrate.

4. A method of producing a semiconductor device comprising the steps of forming a metallization film (18) including copper on a surface of a substrate (10,12,14,16) and depositing an insulating film (20) on said surface including said metallization film, characterized in that said step of depositing said insulating film (20) is performed by a radio frequency sputtering.

5. A method of producing a semiconductor device as claimed in claim 4, characterized in that said radio frequency sputtering is carried out at a temperature of 200°C or lower.

6. A method of producing a semiconductor device as claimed in any of claims 4 and 5, characterized in that said insulating film is made of a material selected from the group consisting of silicon dioxide, phosphor-silicate glass and silicon nitride.

7. A method of producing a semiconductor device as any of claims 4 to 6, characterized in that said method further comprises the step of annealing said semiconductor device having said insulating film deposited on said substrate.

8. A method of producing a semiconductor device comprising the steps of forming a metallization film (18) including copper on a surface of a substrate (10,12,14,16) and depositing an insulating film (20) on said surface including said metallization film, characterized in that said step of depositing said insulating film (20) is performed by an electron cyclotron resonance plasma-assisted chemical vapor deposition.

9. A method of producing a semiconductor device as claimed in claim 8, characterized in that said electron cyclotron resonance plasma-assisted chemical vapor deposition is carried out at a temperature of 200°C or lower.

10. A method of producing a semiconductor device as claimed in any of claims 8 and 9, characterized in that said insulating film is made of a material selected from the group consisting of silicon nitride and silicon dioxide.

11. A method of producing a semiconductor device as claimed in any of claims 8 to 10, characterized in that said method further comprises the step of annealing said semiconductor device having said insulating film on said substrate.

12. A method of producing a semiconductor device comprising the steps of forming a metallization film (18) including copper on a surface of a substrate (10,12,14,16) and depositing an insulating film (20) on said surface including said metallization film, characterized in that said step of depositing said insulating film (20) is performed by a plasma-assisted chemical vapor deposition.

13. A method of producing a semiconductor device as claimed in claim 12, characterized in that said plasma-assisted chemical vapor deposition is carried out at a temperature of 200°C or lower.

14. A method of producing a semiconductor device as claimed in any of claims 12 and 13, characterized in that said insulating film is made of a material selected from the group consisting of silicon dioxide, phosphor-silicate glass and silicon nitride.

15. A method of producing a semiconductor device as claimed in any of claims 12 to 14, characterized in that said method further comprises the step of annealing said semiconductor device including said metallization film on said substrate.

FIG. 1A

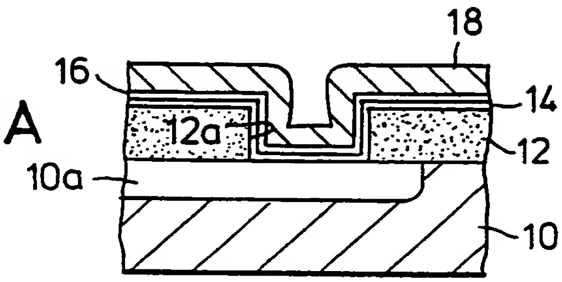


FIG. 1B

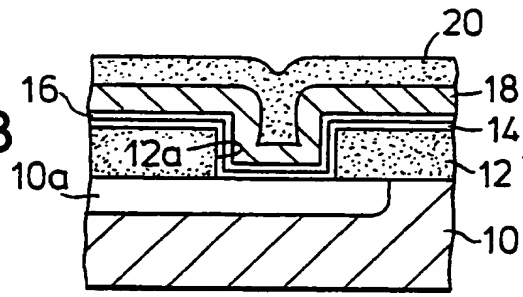


FIG. 1C

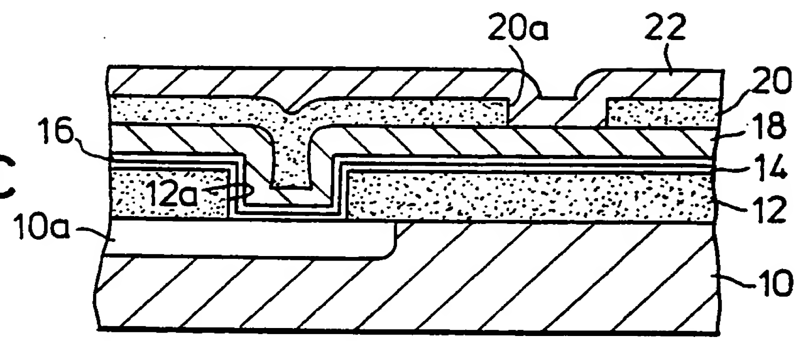


FIG. 1D

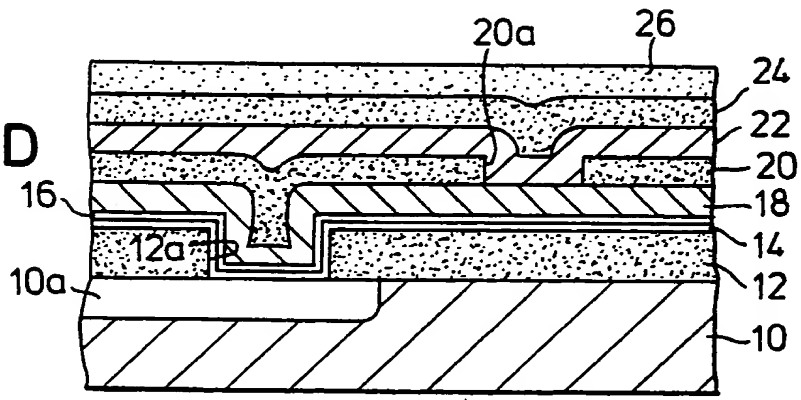
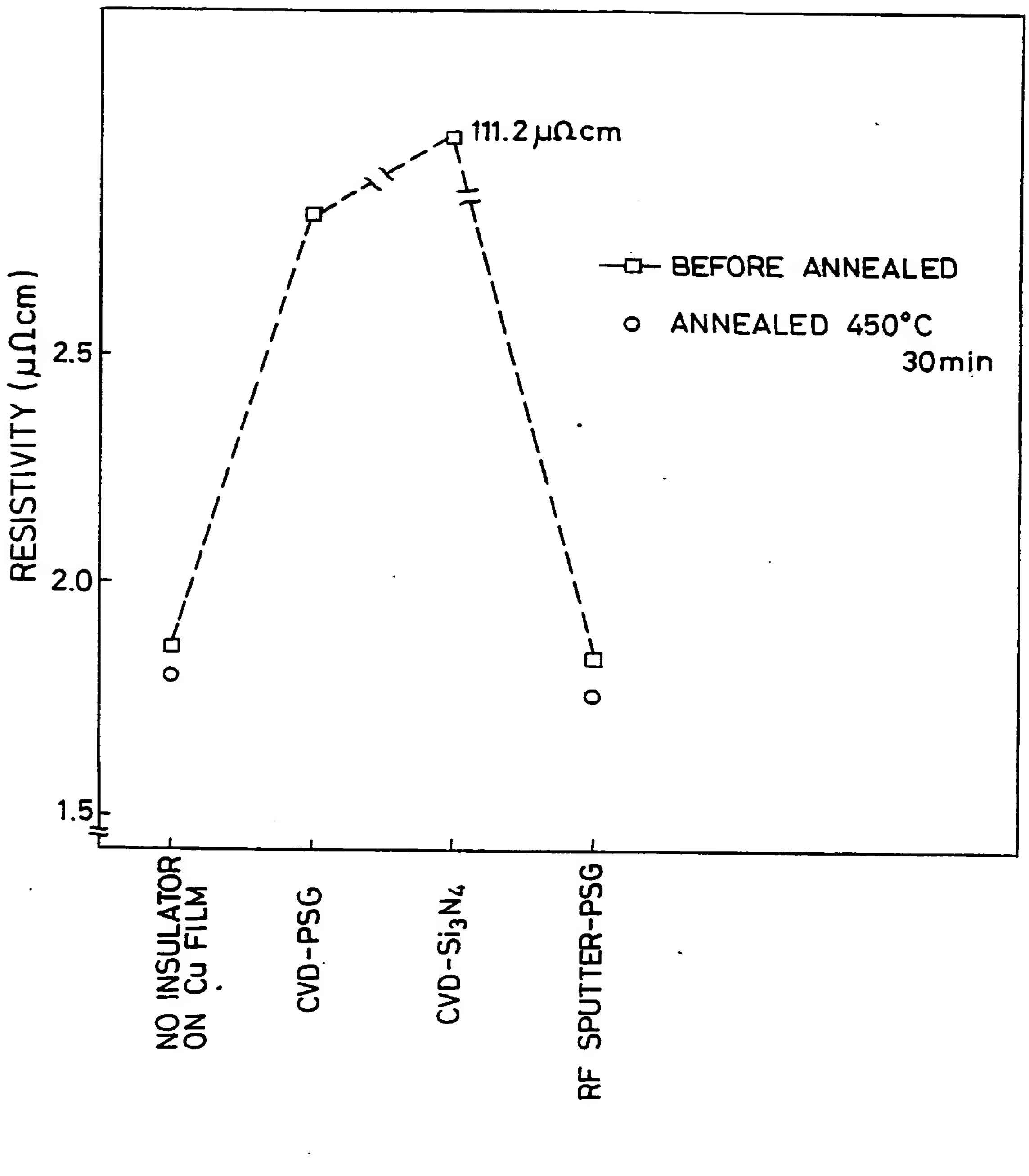


FIG. 2



111.2 µΩcm
BEFORE ANNEALED
ANNEALED 450°C
30min
RESISTIVITY (µΩcm)
2.5
2.0
1.5
NO INSULATOR ON Cu FILM
CVD-PSG
CVD-Si3N4
RF SPUTTER-PSG

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 87 30 8051

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
Y	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 25, no. 3B, August 1982, pages 1677-1680, New York, US; C.Y. TING: "Using A1203 for VLSI multilevel interconnections" * Whole document *	1	H 01 L 21/90 H 01 L 23/52
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Y	EXTENDED ABSTRACTS, Spring Meeting, Toronto, CA., 11th-16th May 1975, vol. 75-1, pages 258-260, abstract no. 112, Electrochemical Soc., Philadephia, US; J.M. MORABITO et al.: "Material characterization of Ti-Cu-Ni-Au (TCNA): a new low cost thin-film conductor system" * Page 258, line 6, from bottom - page 259, line 10 *	1	
A	Idem	2,5,9, 13	**TECHNICAL FIELDS SEARCHED (Int. Cl.4)**

X	US-A-3 725 309 (I. AMES et al.) * Column 4, lines 30-37; figures 2B-1,2B-2; column 7, lines 7-12; column 9, lines 16-23; abstract *	4	H 01 L
A		3,6,7, 10,11, 14,15	
	--- -/-		

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	10-12-1987	MACHEK,J.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
O : non-written disclosure
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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	JAPANESE JOURNAL OF APPLIED PHYSICS SUPPLEMENTS 17th CONFERENCE ON SOLID STATE DEVICES AND MATERIALS, 25th-27th August 1985, pages 329-332, Tokyo, JP; K. MACHIDA et al.: "New planarization technology using Bias-ECR plasma deposition" * Page 329, right-hand column, chapter: "II. Bias-ECR plasma deposition system"; page 330, right-hand column, chapter: "VI. Characteristics of bias-ECR plasma deposition" * ---	8-10	
A	29th ELECTRONIC COMPONENTS CONFERENCE, Cherry Hill, N.J., 14th-16th May 1979, pages 162-169, IEEE, New York, US; R.J. NIKA et al.: "Oxidation kinetics of Cu thin films in air at 100 degrees centigrade to 300 degrees centigrade" * Page 168, right-hand column, chapter "conclusions" * ---	1,2,5,9,13	TECHNICAL FIELDS SEARCHED (Int. Cl.4)
A	PATENT ABSTRACTS OF JAPAN, vol. 5, no. 149 (E-75)[821], 19th September 1981; & JP-A-56 81 952 (HITACHI SEISAKUSHO K.K.) 04-07-1981 * Whole document * -----	6,10,14	

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	10-12-1987	MACHEK, J.

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